

INTRODUCTION

- PCB-based readout electronics is bulky and less optimized
- Discrete components consume more power
- ASIC readout provides optimized function with **more compactness** and **less power consumption**

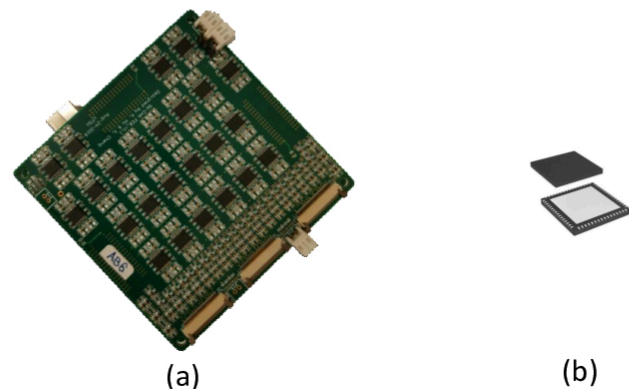


Figure 1: PCB-based readout vs ASIC. (a) Our lab developed 96-channel SiPM Readout Front-ended board; (b) Proposed ASIC with 16-channel

OBJECTIVES

- To design a **multi-channel dual-polarity** ASIC readout chip (SiPMROC, Figure 2) for TOF-PET detectors
- To evaluate the functionality and performance of SiPMROC

METHODS

- 16 energy measurement channels and a summing channel
- Linear-discharging integration circuits [1][2] with improved **gated Baseline-Holder** [3], shown in Figure 3
- Fast current discriminator [4]
- Leading edge discriminator for timing pickoff
- **Digital** control of logic and energy process core
- LVDS transmitters for data and timing output
- **Capable** for a cascaded multiple ASIC readout

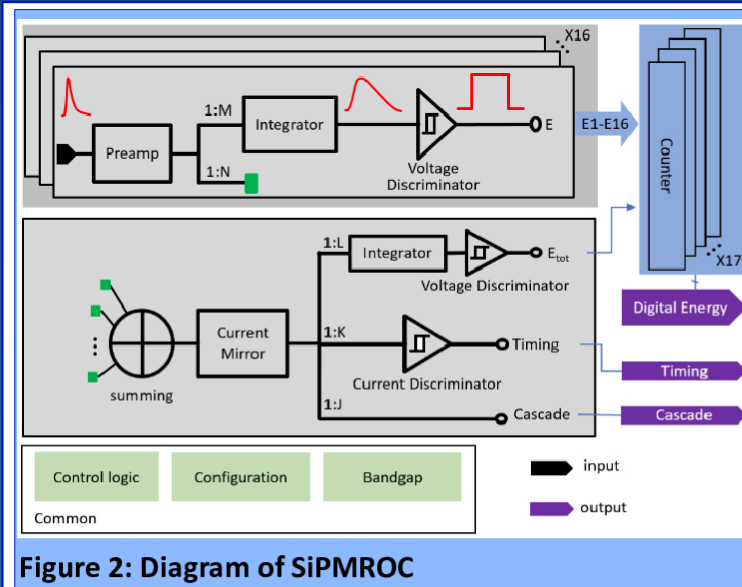


Figure 2: Diagram of SiPMROC

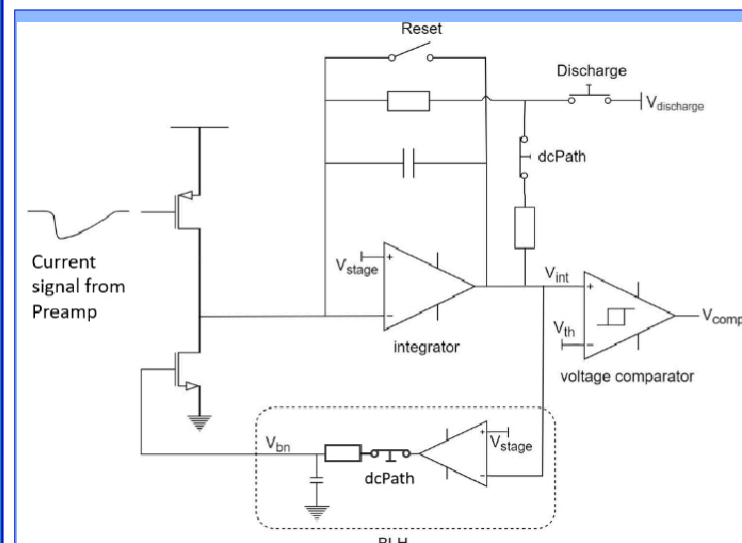


Figure 3: Diagram of Integrator

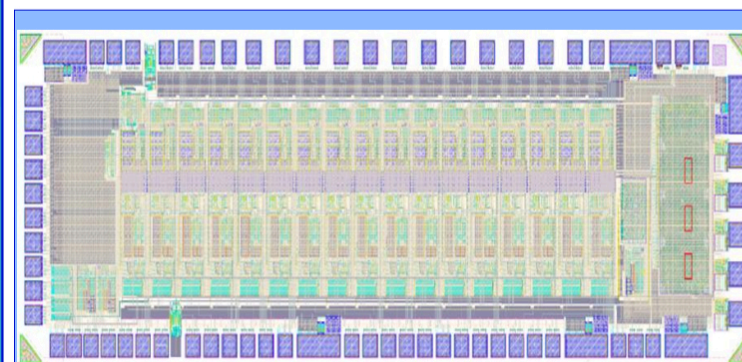


Figure 4: Layout of SiPMROC



Figure 5: Illustration of readout sequence

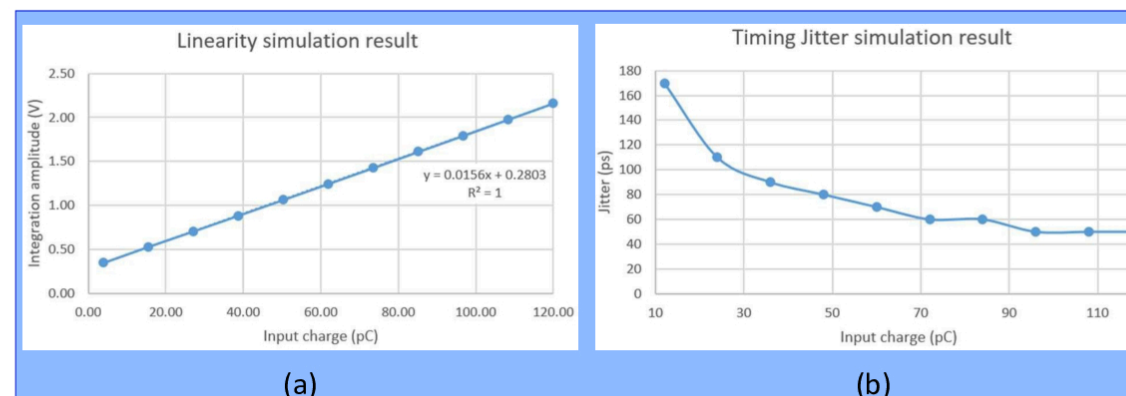


Figure 6: Simulated (a) Linearity of Energy (b) Jitter of Timing measurement

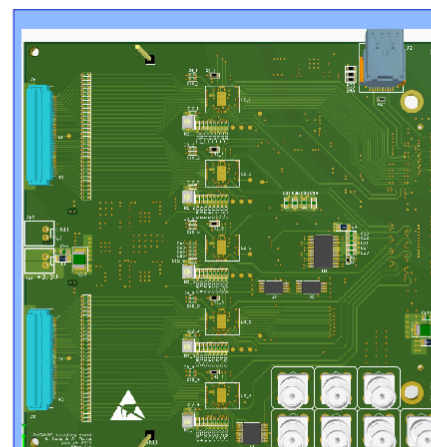


Figure 7: Testing board layout

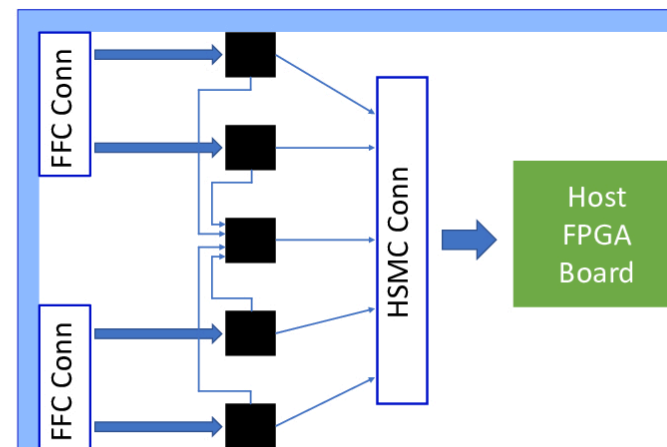


Figure 8: Diagram of Testing board

RESULTS

- 16-channel dual-polarity readout circuits
- 65 nm fab technology, Die size: $1 \times 3 \text{ mm}^2$
- 10 mW/channel (reduced 50% than lab FEB)
- Negligible energy non-linearity and less than 170 ps timing jitter
- Counting rate $\geq 1 \text{ Mevent/s}$
- Dynamic range: 100 fC to 400 pC
- Automatically run after configuration

CONCLUSIONS AND FUTURE WORK

- The multi-channel dual-polarity SiPM readout ASIC has been Fabricated
- Testing board has been designed and is under fabrication
- Will test the functionality and performance of ASIC prototype with LYSO crystals and 8X8 SiPM array

REFERENCES

- [1] Z. Zhao et al., "A novel read-out electronics design based on 1-bit sigmadelta modulation," IEEE Trans. Nucl. Sci., vol. 64, no. 2, pp. 820–828, Feb. 2017.
- [2] X. Cheng, K. Hu and Y. Shao, "Dual-Polarity SiPM Readout Electronics Based on 1-bit Sigma-Delta Modulation Circuit for PET Detector Applications," IEEE Trans. Nucl. Sci., vol. 66, no. 9, pp. 2107-2113, Sept. 2019.
- [3] F. Corsi et al., "ASIC development for SiPM readout," JINST 4 P03004, Mar. 2009
- [4] Z. Deng, A. K. Lan, X. Sun, C. Bircher, Y. Liu and Y. Shao, "Development of an Eight-Channel Time-Based Readout ASIC for PET Applications," in IEEE Transactions on Nuclear Science, vol. 58, no. 6, pp. 3212-3218, Dec. 2011.222

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